The Design of a Low Loss, High Power, Microwave Switch MMIC

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Abstract

This paper describes the development of a low loss, high power, microwave switch MMIC design. The operating bandwidth of the switch was 7 to 11GHz. Simulated performance shows an insertion loss of 0.71dB at mid-band rising to 0.85dB at the band-edge. The estimated power handling capability of the switch is 6.3W at 1dB compression for 0/-10V control. Isolation is better than 27dB across the entire band and the worse-case return loss is 16dB. The design was undertaken using the FD05 0.5μm gate length PHEMT process from Filtronics, which means that the resultant switches would be available from a UK supplier.

Introduction

Compact microwave switches are commercially available as standard product Monolithic Microwave Integrated Circuits (MMICs). However, the losses tend to be relatively high (in the region of 1.5dB at 10GHz) and the power handling capability relatively low (typically less than +27dBm). This paper describes the development of a novel MMIC based microwave switch design that simultaneously offers low insertion loss and high power handling capability. The operating frequency range was 7 to 11GHz. The work assumes the use of the FD05 0.5μm gate length Pseudomorphic High Electron Mobility Transistor (PHEMT) process of Filtronics. This means that any switches fabricated using the design developed, would be available from a UK source.

Development of the Switch Topology

When used as RF switching devices, the transistors of modern PHEMT processes typically have an on-state resistance in the region of 1.5Ω.mm and an off-state capacitance in the region of 03 to 0.5pF/mm. This results in a low insertion loss in the on-state but in the off-state the isolation is limited by the capacitance. A comprehensive introduction to the design of FET and PHEMT based switches can be found in [1].

Many commercially available microwave switch MMICs make use of both series and shunt devices in combination. It is the use of the series devices that makes very low switch losses difficult to realise at microwave frequencies. This is because in choosing a series device that has a low enough off-state capacitance to provide isolation at microwave frequencies, the device is so small that its on-state resistance (and so RF losses) are significant.

In order to realise a switch with the lowest possible insertion loss, it was decided to adopt a topology based around shunt transistors only. A schematic of the basic switching arm that was used is shown in Figure 1. When the shunt mounted PHEMT devices are in the off-state, their shunt capacitance is absorbed into a Low Pass Filter (LPF) structure (hence the series inductors). This allows a very low loss on-case for the switching arm. When the PHEMTs are in the on-state, their low shunt resistance attenuates RF signals so resulting in a high loss (isolation) off-case switching arm. The values of the series inductors required for a microwave frequency LPF are very low, which means that the inductors can be realised on a MMIC as short lengths of transmission line.

In addition to allowing a low loss on-case switching arm, the avoidance of series devices of modest gate width also allows improved power handling. The power handling can be further improved by the use of multiple shunt devices in cascade [1]. The basic switching structure depicted in Figure 1 is a simple SPST switch. However, by ensuring that the input impedance impedance in the off-case is high, two or more such structures can be connected at a common input to realise a multi-way switch. The resulting circuit will be band-pass rather than operating down to baseband, as is normally the case with switch MMICs that also incorporate series devices.

However, it should have much lower losses and higher power handling capability.

The following parameters were investigated to determine the optimum switch topology:

- Choice of filter structure
- Trade-off of number of cascaded shunt devices
- Trade-off of number of switching stages (the order of the filter)

Three different LPF structures were considered: Butterworth, Tchebyscheff and "Optimised". In all cases a 5th order filter was used as the starting point for comparison. The values of the components for a given system impedance and filter cut-off frequency can be readily calculated for both Butterworth and Tchebyscheff filters [2]. The optimised filter was simply a 5th order LC ladder, the component values of which were determined by optimisation.

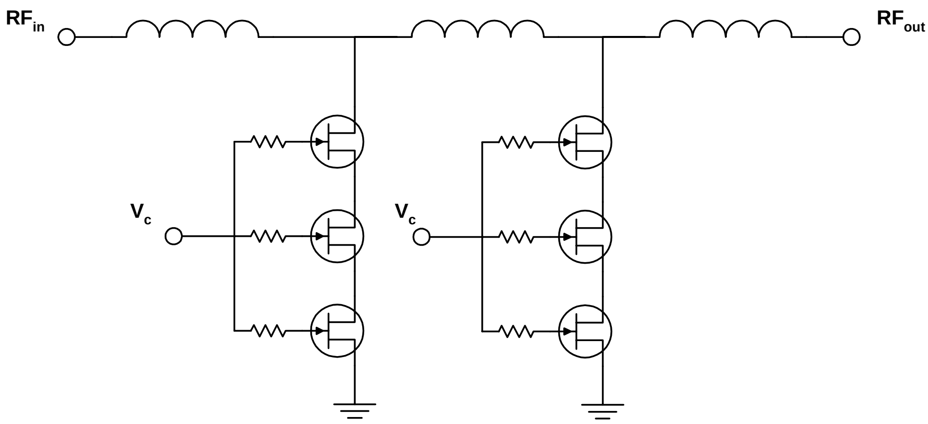

Figure 1: Basic Switch Topology

The shunt capacitors of the LPF were replaced with PHEMTs of appropriate gate width. The larger the capacitor, the larger (wider gate width) the PHEMT device that replaces it. The series inductors of the filter structure were then replaced with short lengths of microstrip transmission line. SPDT switches, based on each of the filter structures, were then formed by joining two of the filters at a common input port. The lengths and widths of the series transmission lines, were now optimised for each of the three variants of the switch.

Comparison between the SPDTs realised using the three different types of filter structure revealed that the Butterworth based design yielded the best performance. However, the differences between the three were actually very small and any of the filter structures could have been used as the basis for a switch design.

These comparisons of filter structure were undertaken with a stack of three shunt PHEMTs in cascade replacing each shunt capacitor of the LPF (as depicted in Figure 1). The trade-offs associated with the number of cascaded devices used to replace each shunt capacitor were considered next. A switch based on a fifth order Butterworth filter was assumed and cascades of 1 to 5 shunt PHEMTs were considered. This analysis revealed that the best small signal performance is offered by a single device. As more shunt devices are used the insertion loss of the switch increases and the isolation degrades. However, the higher the number of shunt devices used the higher will be the power handling capability of the switch. As the aim of this design work was to develop a switch topology capable of offering both high power handling and low insertion loss, a cascade of two shunt PHEMT devices was selected as the most appropriate compromise.

The order of the filter on which the switch design is based can be readily increased (or decreased) with the trade-off that switches based on higher order filters will have higher off-state isolation but increased on-state insertion loss. An assessment of the magnitude of these trade-offs was the next stage of the design process. Switch designs based on Butterworth filters of 3rd, 5th and 7th order were considered. It was concluded that the 5th order design was most appropriate.

Final Switch Design Optimisation

The preliminary design work detailed above determined that the switch design should be based on a 5th order Butterworth LPF with a cascade of two shunt PHEMT devices replacing each shunt capacitor. An assessment was now made of other enhancements to the design that could be considered. The following modifications were found to offer some modest performance benefit:

- Increasing the metallisation thickness
- Increasing the value of the gate bias resistors
- Including series matching capacitors

Large signal (power handling) performance

In order to simulate how the performance of the switch varies with input power level, an accurate large signal model is required. Large signal models are available for the FD05 process that are well suited to predicting the large signal performance of amplifying transistors but these are unlikely to provide accurate predictions of the performance of circuits in which the transistors are used as switches. It is possible, however, to make reasonable estimates of the expected compression performance from the breakdown voltage and saturated current capacities of the transistors used [1].

For the switch topology under consideration, compression will occur in the off-state devices due to the RF voltage being sufficient to move the devices out of pinch-off or into breakdown. The input power levels that will cause this effect to occur are dependent on the control voltages used. Two cases are considered: 0/-7.5V control and 0/-10V control. The estimated 1dB compression points were +35dBm (or 3.2W) for –7.5V control and +38dBm (or 6.3W) for –10V control.

Summary of Simulated Performance

The final schematic of the optimised switch topology is shown in Figure 2. The final simulated performance is shown in Figure 3 and Figure 4. A summary of the final simulated performance of the switch is shown in Table 1. The insertion loss is 0.71dB at mid-band rising to 0.85dB at the band-edge. The estimated power handling capability is 6.3W for 0/-10V control, and 3.2W for 0/-7.5V control. Isolation is better than 27dB across the entire 7-11GHz band and the worse-case return loss is 16dB.

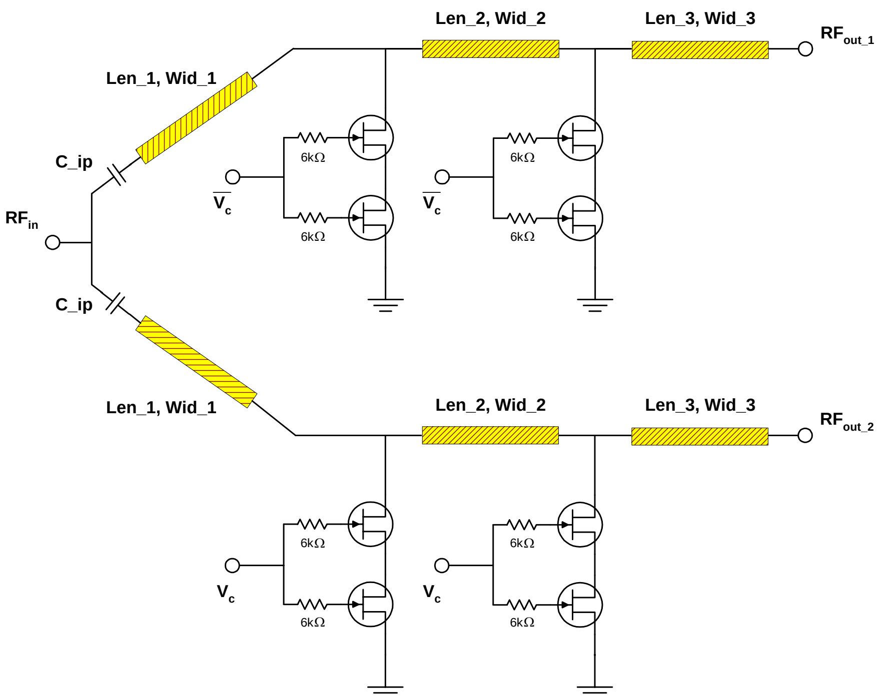

Figure 2: schematic of the optimum SPDT switch topology

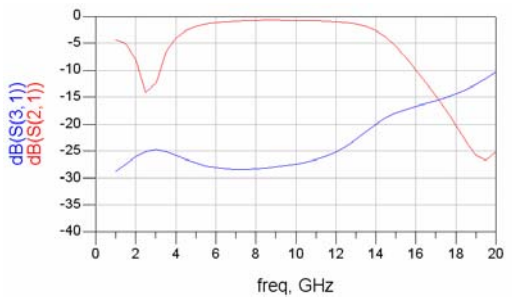

Figure 3: Final simulated SPDT performance

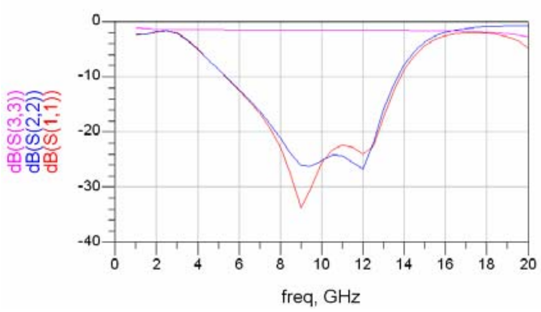

Figure 4: Final simulated SPDT performance

Parameter	Units	Mid-band	Worse-case 7-11GHz
Insertion loss	dB	0.71	0.85
Isolation	dB	28	27
Input return loss	dB	34	17
Output return loss (on-state)	dB	26	16
P-1dB (0/-7.5V control)	W	3.2	3.2
P-1dB (0/-10V control)	W	6.3	6.3

Table 1: Summary of simulated performance for the final SPDT

Conclusions

This paper has detailed the development of a low loss, high power, microwave SPDT switch MMIC design. The design approach was based on using shunt mounted transistors only (to avoid the insertion loss associated with series devices) incorporated into a low pass filter structure. The FD05 PHEMT process of Filtronics was used, which ensures a UK source of the resulting design. The findings of the work were:

- The switch design should be based on a Butterworth LPF (although there was very little to choose between this and a Tchebyscheff based design).
- A cascade of two shunt PHEMT devices should be used to replace each shunt capacitor in the filter as this offers the best compromise between low insertion loss and high power handling.
- A 5th order filter offers acceptable isolation and lowest insertion loss.
- The thickest microstrip transmission lines allowed by the process should be used in order to minimise insertion loss.
- High value gate bias resistors should be used.
- Series input matching capacitors in each arm of the switch can offer modest performance benefits.
- Although good performance is demonstrated across the primary band of 7 to 11GHz, the topology investigated is not well-suited to the realisation of wider-band switches.
- The use of a 0.25µm gate length PHEMT process could offer further reductions in insertion loss but any associated reduction in breakdown voltage would degrade the power handling capability.

Acknowledgements

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References

[1] Devlin, Liam "The Design of Integrated Switches and Phase Shifters", Proceedings of the IEE Tutorial Colloq. on "Design of RFICs and MMICs", Wednesday 24th November 1999, pp 2/1-14

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